PAIDC

QUERY CONTROL FORM				RTIS USE ONLY	
Application No.	09/897,158	Prepared by	NH	Tracking Number	05903949
Examiner-GAU	Wille - 2814	Date	3-17-4	Week Date	02/16/04
		No. of queries	2	IFW	

JACKET			
a. Serial No.	f. Foreign Priority	k. Print Claim(s)	p. PTO-1449
b. Applicant(s)	g. Disclaimer	l. Print Fig.	q. PTOL-85b
c. Continuing Data	h. Microfiche Appendix	m. Searched Column	r. Abstract
d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs
e. Domestic Priority	j. Claims Allowed	o. PTO-892	t. Other

SPECIFICATION

a. Page Missing
b. Text Continuity
c. Holes through Data
d. Other Missing Text
e. Illegible Text
f. Duplicate Text
g. Brief Description
h. Sequence Listing
i. Appendix
j. Amendments
k. Other

CLAIMS

a. Claim(s) Missing
b. Improper Dependency
c. Duplicate Numbers
d. Incorrect Numbering
e. Index Disagrees
f. Punctuation
g. Amendments
h. Bracketing
i. Missing Text
j. Duplicate Text
k. Other

MESSAGE

① Claims 3-4 (originally claims 7 and 8, respectively) depends on claim 7 (originally claim 6. Please Advise and correct claim dependency.

② Claim 6 (now claim 7) depends on claim 11. Please Advise and correct claim dependency.

Thankyou

initials NH

RESPONSE

Index corrected.

CLM PTO supplied (best available copy) with claims & dependences renumbered according to index.

initials JBH

ISSUE SLIP STAPLE AREA (for additional cross references)

POSITION	INITIALS	ID NO.	DATE
FEE DETERMINATION			
O.I.P.E. CLASSIFIER			
FORMALITY REVIEW	CJ	1122	08/21/01
RESPONSE FORMALITY REVIEW			

INDEX OF CLAIMS

✓ ..... Rejected
= ..... Allowed
– (Through numeral)... Canceled
÷ ..... Restricted
N ..... Non-elected
I ..... Interference
A ..... Appeal
O ..... Objected

Claim		Date
Final	Original	
	1	✓
	2	✓
	3	✓
1	4	O
2	5	O
5	6	✓
6	7	✓
7	8	✓
10	9	O
13	10	O
14	11	O
17	12	✓
	13	
	14	
	15	
	16	
	17	✓
	18	
	19	✓
3	20	–
4	21	
8	22	
9	23	
11	24	
12	25	
15	26	
16	27	=
	28	
	29	
	30	
	31	
	32	
	33	
	34	
	35	
	36	
	37	
	38	
	39	
	40	
	41	
	42	
	43	
	44	
	45	
	46	
	47	
	48	
	49	
	50	

Claim		Date
Final	Original	
	51	
	52	
	53	
	54	
	55	
	56	
	57	
	58	
	59	
	60	
	61	
	62	
	63	
	64	
	65	
	66	
	67	
	68	
	69	
	70	
	71	
	72	
	73	
	74	
	75	
	76	
	77	
	78	
	79	
	80	
	81	
	82	
	83	
	84	
	85	
	86	
	87	
	88	
	89	
	90	
	91	
	92	
	93	
	94	
	95	
	96	
	97	
	98	
	99	
	100	

Claim		Date
Final	Original	
	101	
	102	
	103	
	104	
	105	
	106	
	107	
	108	
	109	
	110	
	111	
	112	
	113	
	114	
	115	
	116	
	117	
	118	
	119	
	120	
	121	
	122	
	123	
	124	
	125	
	126	
	127	
	128	
	129	
	130	
	131	
	132	
	133	
	134	
	135	
	136	
	137	
	138	
	139	
	140	
	141	
	142	
	143	
	144	
	145	
	146	
	147	
	148	
	149	
	150	

If more than 150 claims or 10 actions staple additional sheet here

(LEFT INSIDE)

569 8/21/01

11. (Amended) A method of creating a hybridized chip combining a top active optical device chip, having a substrate including a first side and active device contacts on top active devices located on the first side, the top active optical devices also being on the first side, with an electronic chip having electronic chip contacts, when at least some of the active device contacts are not aligned with at least some of the electronic chip contacts when the top active optical device chip and the electronic chip are superimposed, each of the at least some active device contacts having an electrically corresponding electronic chip contact, the method comprising:

attaching a carrier to the top active optical device;

creating sidewalls defining openings in the substrate extending from the active device contacts on the first side through the substrate to a bottom side of the substrate opposite the first side at points on the bottom side substantially coincident with the active device contacts on the top side;

making the sidewalls electrically conductive to form electrically conductive paths from the active device contacts to the points; and

connecting the points to locations correspondingly aligned with the at least some electronic chip contacts with an electrically conductive material located on the bottom side of the active optical device chip.

25 (Amended) The method of claim 11 further comprising:

removing the carrier after the connecting.

26 (Amended) The method of claim 11 wherein the connecting comprises:

patterning traces between the points and the locations correspondingly aligned with the at least some electronic chip contacts, and

making the traces electrically conductive.

6 7. (Amended) The method of claim 5 6 wherein the patterning traces comprises:

patterning at least some of the traces on the substrate and at least some other of the traces on the electronic chip.

7 8. (Amended) The method of claim 5 6 wherein the patterning traces further comprises:

patterning traces on the electronic chip.

5 9 10 (Amended) A method of creating a hybridized chip combining a top active optical device chip, having a substrate including a first side and active device contacts on top active devices located on the first side, the top active optical devices also being on the first side, with an electronic chip having electronic chip contacts, when at least some of the active device contacts are not aligned with at least some of the electronic chip contacts when the top active optical device chip and the electronic chip are superimposed, each of the at least some active device contacts having an electrically corresponding electronic chip contact, the method comprising:

thinning the substrate;

creating sidewalls defining openings in the substrate extending from the active device contacts on the first side through the substrate to a bottom side of the substrate opposite the first side at points on the bottom side substantially coincident with the active device contacts on the top side;

making the sidewalls electrically conductive to form electrically conductive paths from the active device contacts to the points; and

connecting the points to locations correspondingly aligned with the at least some electronic chip contacts with an electrically conductive material located on the bottom side of the active optical device chip.

13

16. (Amended) A method of creating a hybridized chip combining a top active optical device chip, having a substrate including a first side and active device contacts on top active devices located on the first side, the top active optical devices also being on the first side, with an electronic chip having electronic chip contacts, when at least some of the active device contacts are not aligned with at least some of the electronic chip contacts when the top active optical device chip and the electronic chip are superimposed, each of the at least some active device contacts having an electrically corresponding electronic chip contact, the method comprising:

attaching a carrier having a thickness greater than a minimum lasing thickness over the top active device;

creating sidewalls defining openings in the substrate extending from the active device contacts on the first side through the substrate to a bottom side of the substrate opposite the first side at points on the bottom side substantially coincident with the active device contacts on the top side;

making the sidewalls electrically conductive to form electrically conductive paths from the active device contacts to the points; and

connecting the points to locations correspondingly aligned with the at least some electronic chip contacts with an electrically conductive material located on the bottom side of the active optical device chip.

~~14~~ ~~11~~. The method of claim ~~10~~ 13 further comprising:

patterning access ways in the carrier and applying an anti-reflection coating to the carrier.

17 (Amended) A hybridized chip comprising:

at least one top active optical device coupled to an electronic chip, the hybridized chip having been created using the method of one of claims 1-16.

3

~~20~~ The method of claim ~~2~~ 1 further comprising:

thinning the substrate.

~~21~~ 4

~~21~~ The method of claim ~~2~~ 1 further comprising:

thinning the substrate.

6 22. The method of claim 1, 2, 3, 4, 5, 20 or 21 further comprising attaching a carrier having a thickness greater than a minimum lasing thickness over the top active device.

9 23. The method of claim 8 further comprising:

patterning access ways in the carrier and applying an anti-reflection coating to the carrier.

Cancel

11 24. The method of claim 10 further comprising attaching a carrier having a thickness greater than a minimum lasing thickness over the top active device.

12 25. The method of claim 11 further comprising:

patterning access ways in the carrier and applying an anti-reflection coating to the carrier.

15 26. The method of claim 1, 2, 10, 13, 14, 3, 4, 11 12 wherein the making the sidewalls electrically conductive comprises:

filling at least some of the openings with an electrically conductive material.

16 27. The method of claim 1, 2, 10, 13, 14, 3, 4, 11 12 wherein the making the sidewalls electrically conductive comprises:

depositing an electrically conductive material on at least some of the sidewalls.--